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Performance and Stability of Aerosol-Jet-Printed Electrolyte-Gated Transistors Based on Poly(3-hexylthiophene)

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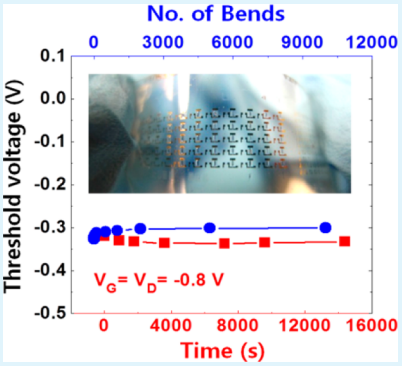
Supporting Information

ABSTRACT: We report performance optimization and stability analysis of aerosol-jet-printed electrolyte-gated transistors (EGTs) based on the polymer semiconductor poly(3-hexylthiophene) (P3HT). EGTs were optimized with respect to printed P3HT thickness and the completed device annealing temperature. EGTs with relatively thin P3HT films (~50 nm) annealed at 120 °C have the best performance and display an unusual combination of metrics including sub-1-V operation, ON/OFF current ratios of 10^6, OFF currents of $<10^{-10}$ A ($<10^{-6}$ A cm^{-2}), saturation hole mobilities of 1.3 cm^2 V^{-1} s^{-1}, threshold voltages of −0.3 V, and subthreshold swings of 70 mV decade^{-1}. Furthermore, optimized EGTs printed on polyester substrates are extremely robust to bias stress and repeated mechanical bending strain. Collectively, the results suggest that optimized P3HT-based EGTs are promising devices for printed, flexible electronics.



KEYWORDS: *electrolyte gating, electrochemical transistor, aerosol jet printing, poly(3-hexylthiophene), ion gel, device stability*

1. INTRODUCTION

Electrolyte-gated transistors (EGTs) have well-recognized potential as chemical sensors, and they may also be useful in printed electronics, because of their inherently low voltage operation, which is compatible with thin film battery power supplies.[1−10] From a processing perspective, an additional attractive feature of EGTs is that the low-frequency capacitance of the electrolyte layer, which serves as the gate insulator, is not dependent on the layer thickness, meaning that relatively thick layers (e.g., 1 μm) can be printed easily and without pinholes; low-voltage operation is maintained. Demonstrations of EGT-based circuits include low voltage inverters, ring oscillators, NAND gates, and D flip-flops.[11−13] However, further development of practical applications of EGTs naturally requires a thorough understanding of their performance and stability limits. In the present study, we have investigated the performance and stability of printed *p*-type EGTs employing poly(3-hexylthiophene) (P3HT) as the semiconductor channel material and "ion gels" as the gate electrolyte layer. These devices are also known as electrochemical transistors, because ions from the electrolyte penetrate into the P3HT layer, causing reversible electrochemical oxidation to the conducting ON state during operation. The detailed operation mechanisms of EGTs have been described in recent reviews.[13,14]

We demonstrate here that optimized P3HT EGTs have many very favorable performance characteristics, including sub-1-V operation, ON/OFF current ratios of 10^6, threshold voltages (V_{th}) slightly negative of 0 V, static leakage currents of $<10^{-6}$ A cm^{-2}, and subthreshold swings (SS) of <70 mV decade^{-1}. These results were obtained after systematic optimization of the device architecture and fabrication procedure, as described below, and they represent a significant improvement over our prior reports.[3,11,15] In addition, we show that printed EGTs on plastic are extremely robust to bias stress for up to 4 h of continuous operation and to repeated mechanical bending operations at 1.5% maximum strains. We are currently aware of only one previous study on the stability of EGTs (i.e., ZnO-based EGTs), with respect to bias stress and mechanical strain.[14]

2. EXPERIMENTAL SECTION

Materials. P3HT was purchased from Rieke Metals and used without any further purification. To prepare the semiconductor ink, P3HT (~1 mg/mL) was dissolved in a solvent mixture of chloroform and terpineol (9:1 by weight). The ion gel ink was composed of 1.0 wt % polystyrene-b-poly(methylmethacrylate)-b-poly(styrene) (PS-PMMA-PS) (Mn = 8.9k − 67k − 8.9k) and 9 wt % of ionic liquid ((1-ethyl-3-methylimidazolium bis(trifluoromethylsufonyl)amide [EMIM][TFSA], Merck) in ethyl acetate solution. The commercially available poly(3,4-ethylenedioxythiophene) poly(styrenesulfonate) (PEDOT:PSS) ink (PH 500, 1.5 wt % polymer in deionized water, from H.C. Starck) was diluted with 10% (by volume) of ethylene glycol to enhance the conductivity.

Device Fabrication. Source and drain electrodes for P3HT EGTs were patterned by photolithography and were completed by e-beam evaporation of Cr (2 nm)/Au (28 nm) on SiO_2 and polyethylene

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terephthalate (PET) substrates. The width and length of the channels were 500 and 25 μm, respectively. Printing of P3HT, ion gel and PEDOT:PSS inks was accomplished in ambient conditions using a commercially available aerosol-jet printing system (Optomec, Inc.). Substrates were heated to 60 °C during printing and the printing speed and nozzle diameter size were fixed at 1 mm s^{-1} and 150 μm for all cases, respectively. The flow rates of carrier and sheath gas for each ink were, respectively, 15 and 25 sccm for P3HT, 9 and 35 sccm for the ion gel, and 20 and 30 sccm for PEDOT:PSS. Completed devices were thermally annealed at various temperatures for 30 min in a N_2-filled glovebox (below 1 ppm O_2 content), unless specified otherwise. The thickness and surface morphology of P3HT films were measured by a surface profiler (KLA-Tencor P-16) and an atomic force microscopy (AFM) system (Bruker Nanoscope V Multimode with QNM), respectively.

Electrical Measurements. The electrical characterization of P3HT devices were accomplished using two computer-controlled Keithley 236 source-measure units and a Keithley 6517 electrometer in an N_2-filled glovebox at room temperature.

3. RESULTS AND DISCUSSION

Figure 1a describes the aerosol-jet printing process for the fabrication of EGTs. The P3HT semiconductor, the ion gel

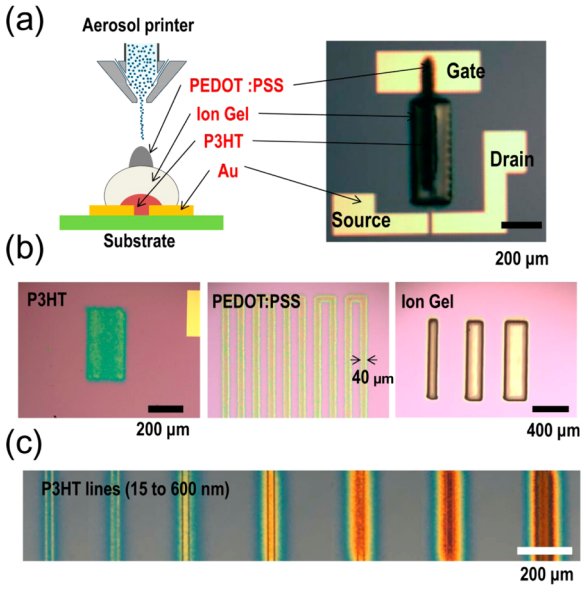

Figure 1. (a) Scheme of the aerosol-jet printing process for fabrication of P3HT EGT devices (left image) and overall device architecture with top-gate, staggered source and drain contacts (right image). Width and length of the channel are 500 and 25 μm, respectively. (b) Optical micrograph of the printed P3HT film (left), PEDOT:PSS (middle), and ion gel electrolyte (right). (c) Thickness-controlled P3HT film in the channel region (15–600 nm) characterized by optical microscopy.

electrolyte, and the PEDOT:PSS gate electrodes were sequentially printed onto SiO_2 or PET plastic substrates prepatterned with gold electrodes. The completed devices have a top gate, staggered source and drain contact architecture with channel width (W) and length (L) of 500 and 25 μm, respectively (Figure 1a, right image). Figures 1b and 1c show the patterning fidelity that can be achieved by aerosol-jet printing of each EGT material.

Figures 2a and 2b display the logarithm of the drain current versus gate voltage (log I_D–V_G) and drain current versus drain voltage (I_D–V_D) characteristics of an optimized printed P3HT EGT on SiO_2. From both plots, it is evident that the device exhibited good linear and saturation behavior at low and high drain voltages, respectively, in the V_D range of 0 to −0.8 V. Figures 2c–f display the statistical spread in key figures of merit for 45 of 45 printed EGTs that were fabricated in one printing session. The average saturation charge carrier mobility (μ) and V_{th} were found to be 1.4 cm^2 V^{-1} s^{-1} and −0.3 V, respectively. For each device, μ and V_{th} were determined from plots of $I_D^{1/2}$ versus V_G, according to the standard saturation regime relation

$$I_D = \mu C_i W (2L)^{-1} (V_G - V_{th})^2$$

where C_i is the capacitance of the gate insulator. The C_i value was estimated from displacement current measurements on each EGT,[16,17] and reached up to 162 μF cm^{-2} for devices with 50-nm-thick P3HT films, as shown in Figure S1 in the Supporting Information (SI). The devices also yielded ON/OFF current ratios of ~10^6 and exhibited very small hysteresis (<10 mV), which we define as the difference in V_G between the OFF-to-ON and ON-to-OFF transfer curves at I_D = 1 μA. In addition, the average SS ($dV_G/d(\log I_D)$) value was 66 mV $decade^{-1}$, approaching the theoretical room-temperature limit of 59 mV $decade^{-1}$.[18] There were no significant differences between individual transistors, implying excellent fabrication reproducibility. The good performance of these devices was achieved by an optimization procedure that is discussed below.

Device performance was first optimized with respect to thickness of the printed P3HT layer. This parameter is particularly important for P3HT EGTs as film thickness controls the diffusion dynamics of the electrolyte ions that must enter and leave the film during switching. The P3HT thicknesses were adjusted from 15 nm to 600 nm by printing (in air) single P3HT lines (height: 15 nm, width: 30 μm) atop one another repeatedly. For all devices, the ion gel and PEDOT:PSS gate layer were printed in air under the same conditions, and a post-annealing process for completed P3HT EGTs was carried out in N_2 atmosphere at 120 °C for 30 min.

Figures 3a and 3b display the thickness dependence of minimum OFF-state and maximum ON-state drain current (I_{OFF} and I_{ON}), hysteresis, and SS, which were extracted from transfer curves of the same devices (e.g., see Figure S2 in the SI). Interestingly, I_{ON} shows a bell-shaped evolution versus thickness with a peak value corresponding to 100-nm-thick P3HT films (Figure 3a). AFM imaging of the surface morphologies for the aerosol-jet P3HT films (see Figure S3 in the SI) reveals that, for printed P3HT films below 20 nm in thickness, individual P3HT clusters with lateral dimensions of ~50 nm are randomly connected on the substrate, but a considerable portion of the surface remains vacant. As the printed P3HT film thickness increases, vacant areas diminish, and the clusters become larger, which leads to a continuous film. The discontinuous morphology characteristic of the thinnest jet-printed P3HT films impedes charge transport, resulting in lower I_{ON} values. Thus, as film thickness initially increases, and coalescence occurs, the channel conductance also increases. The maximum near 100 nm is likely due to contact resistance. That is, for thicker P3HT films, it becomes increasingly difficult to inject charge from the bottom source and drain electrodes into the channel. Further thickness increases beyond 100 nm lead to a drop in I_D.

I_{OFF}, hysteresis, and SS, on the other hand, increase monotonically as P3HT thickness increases (see Figures 3a and 3b). Increasing I_{OFF} with increasing P3HT thickness is reasonable, because I_{OFF} likely reflects residual O_2 doping in the P3HT (the devices are printed in air); therefore, a thicker film

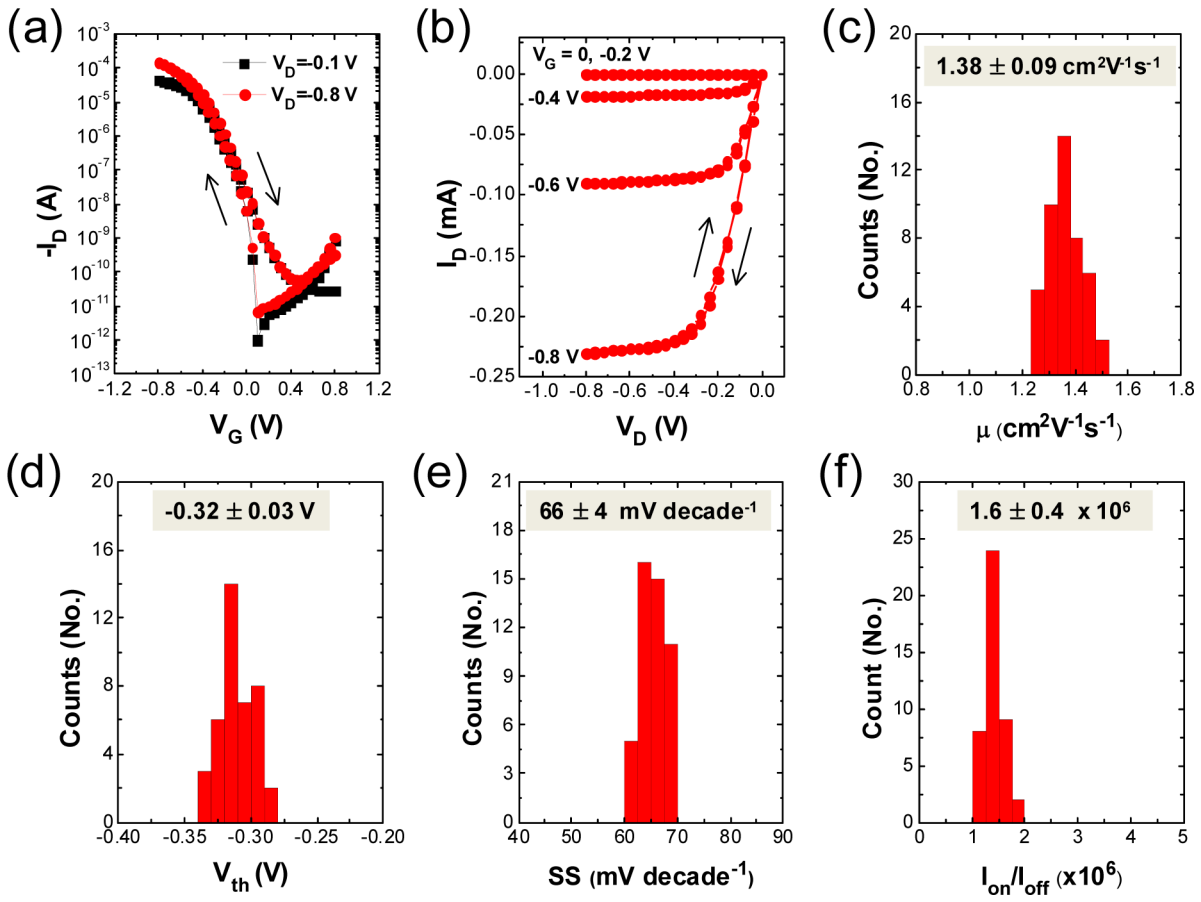

Figure 2. (a) Log I_D−V_G and (b) I_D−V_D characteristics for a printed P3HT EGT on SiO_2 (P3HT thickness is 50 nm). Statistical distributions of the key figures of merit are shown in subsequent panels for 45 printed P3HT EGTs: (c) saturation hole mobility (μ), (d) threshold voltage (V_{th}), (e) subthreshold slope (SS), and (f) ON/OFF current ratio (I_{ON}/I_{OFF}). The gate sweep rate was 100 mV s^{-1}.

will result in more current in the OFF state.[19] Similarly, an increase in hysteresis is expected for thicker P3HT films because ion transport into and out of the film will be impeded, relative to thinner films. Subthreshhold slope SS will also increase with thickness, because of slow ion diffusion in thick P3HT films.

We have also observed that P3HT thickness affects the dynamic performance of the EGTs (Figure 4). In the case of EGTs with 15- and 50-nm-thick P3HT films, I_{OFF}, I_{ON}, hysteresis, and SS remain almost unchanged, with respect to variation in the gate voltage sweep rate by 1 order of magnitude, from 10 mV s^{-1} to 100 mV s^{-1}. In contrast, EGTs with thicker P3HT films (150 and 300 nm) exhibit higher I_{OFF} and larger hysteresis as the gate sweep rate increases. These results are consistent with the scenario that ion diffusion into and out of the P3HT films is important for opening and closing the conducting channel in EGTs. Based on the data in Figures 3a, 3b, and 4, we have concluded that EGTs with ∼50-nm-thick P3HT films are optimum in terms of static and dynamic device performance.

Figures 3c and 3d show the effect of the second optimization parameter, annealing temperature (T_{ann}), on EGT performance. Thermal annealing was carried out in a N_2-filled glovebox (<1 ppm O_2) for 30 min at each temperature after complete device fabrication. We tested annealing effects on EGTs with three different P3HT thicknesses (50, 150, and 300 nm) and the corresponding transfer curves as a function of annealing temperature are shown in Figure S4 in the SI. As T_{ann} increased from 60 °C to 150 °C, all the devices exhibited a negative shift in the turn-on voltages ($V_{turn\text{-}on}$). Here, $V_{turn\text{-}on}$ is defined on the log I_D−V_G plot as the voltage where a sharp increase in current begins (because of this definition, $V_{turn\text{-}on}$ is always slightly more positive of V_{th}, which is defined on a linear plot). The systematic shift in $V_{turn\text{-}on}$ with T_{ann} is potentially useful as a means to tune the threshold voltage for circuit applications. The effect is large: changing T_{ann} from 60 °C to 150 °C results in a negative shift in $V_{turn\text{-}on}$ of 400−500 mV, depending on P3HT film thickness. The cause of this large shift in $V_{turn\text{-}on}$ is not entirely clear. It could be a dedoping effect. As mentioned above, aerosol-jet printing of P3HT in air may lead to entrapment of O_2 in the P3HT, which then *p*-dopes the polymer. Thermal annealing under N_2 may drive out entrapped O_2 by densification and partial crystallization of the P3HT. Indeed, we find that thermal annealing leads to shrinkage of printed P3HT films, which is consistent with densification and crystallization; higher T_{ann} or a thicker P3HT film resulted in larger film shrinkage (see Figure S5 in the SI). P3HT films 300 nm thick underwent film shrinkage of ∼30%.

A denser film morphology upon annealing is also consistent with the hysteresis results (see Figure 3d). We observe that hysteresis in the transfer curves increases with annealing temperature, which can be explained by increased densification leading to slower ion diffusion into and out of the film. The increase in hysteresis with T_{ann} is much more pronounced for thicker films; 300-nm-thick P3HT films have a hysteresis of ∼650 mV when annealed at 120 °C. However, for 50-nm-thick

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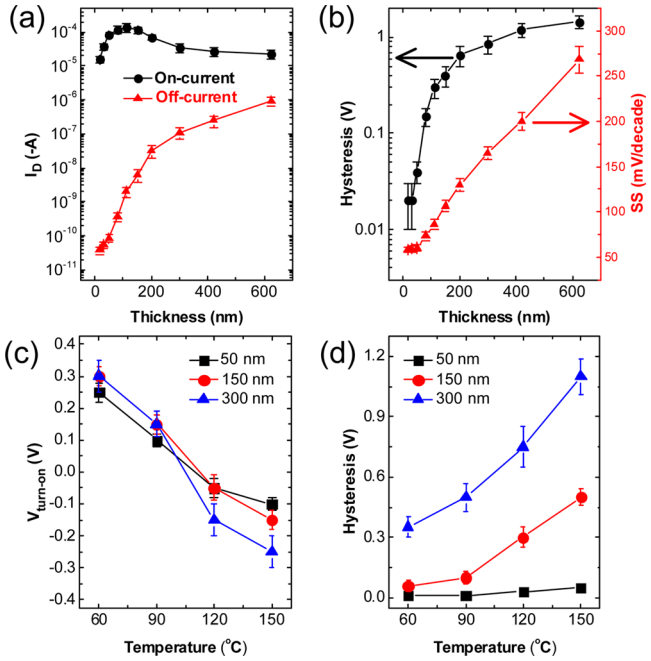

Figure 3. EGT optimization with respect to P3HT layer thickness and annealing temperature. (a) Minimum OFF-state and maximum ON-state drain current (I_{OFF} and I_{ON}), and (b) hysteresis and subthreshold slope (SS) as a function of P3HT thickness for printed P3HT EGTs on SiO_2. These devices were annealed at 120 °C for 30 min. I_{OFF} and I_{ON} were extracted from ON-to-OFF linear-regime transfer curves of each EGT (V_D = −0.1 V). (c) Turn-on voltage ($V_{turn-on}$) and (d) hysteresis as a function of annealing temperature (T_{ann}) for EGTs with different P3HT thicknesses (50, 150, and 300 nm). Error bars represent one standard deviation. Gate voltage sweep rates were 100 mV/s.

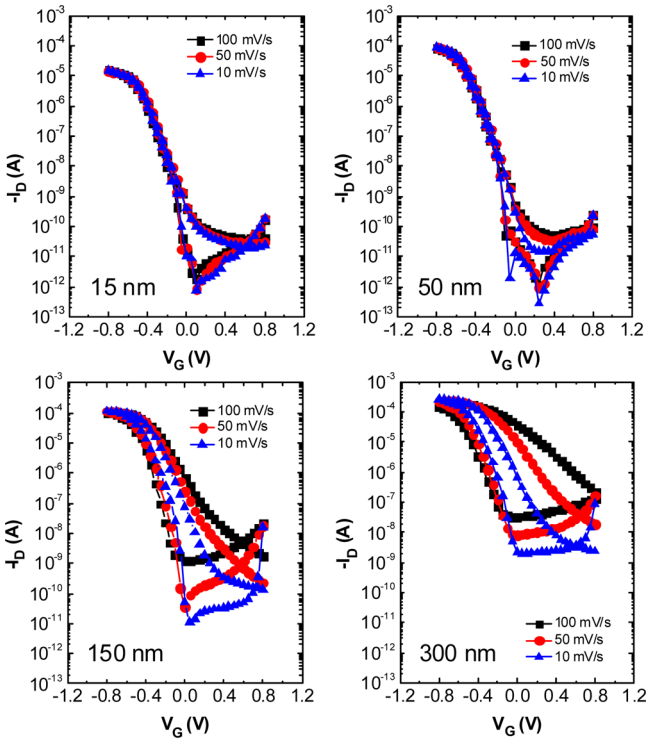

Figure 4. Sweep-rate-dependent I_D−V_G transfer curves for printed EGTs with different P3HT thicknesses (from 15 nm to 300 nm). All devices were annealed at 120 °C. Labels in the lower left of each panel indicate the P3HT thickness employed in the EGT.

films, the hysteresis is only on the order of 10 mV. We note that, generally, thermal annealing of the gate insulator has been employed in the literature to reduce device hysteresis in conventional organic thin film transistors (OTFTs); the proposed mechanisms for improved hysteresis upon annealing include removing H_2O and solvent molecules from the gate dielectric, or fixing polar functional groups by densification of the insulator.[20,21] In contrast, our P3HT EGTs show enlarged hysteresis with increasing T_{ann}, particularly for thick P3HT films, which we believe is due to slower ion diffusion into the densified semiconductor film, as noted above. Based on the data in Figures 3c and 3d, we believe that 120 °C is the optimum T_{ann} as it places V_{th} slightly negative of 0 V (so that, at 0 V, the device is fully OFF), while keeping the hysteresis quite small.

With optimized EGTs in hand, we have investigated the stability of the devices on SiO_2 with respect to bias stress. Bias stress refers to the empirical phenomenon in which a shift in V_{th} occurs upon application of the gate bias for extended periods of time, either continuously or with a heavy-duty cycle. Bias stress has been observed frequently in OTFTs,[22,23] and it is often ascribed to charge trapping in the semiconductor or insulator films, or at the semiconductor/insulator interface.[22,23] Figures 5a and 5b show time-dependent I_D decay under constant bias stress for printed P3HT EGTs, as a function of the P3HT thickness and annealing temperature, respectively. Each EGT was fabricated on SiO_2 with the same ion gel and PEDOT:PSS layers and annealed for 30 min under N_2 before measurement. The devices were tested under N_2 by applying sustained biases of V_G = V_D = −0.8 V for a period of 1 h.

As shown in Figure 5a, the 15-nm-thick P3HT EGT (annealed at 120 °C) on SiO_2 exhibits an I_D decay of 7% after 1 h of bias stressing. The extent of I_D decay decreases with increasing P3HT thickness, however, and is only 2%−3% after 1 h for the 150-nm-thick device (which was also annealed at 120 °C). These results suggest a higher degree of charge trapping in the thinner P3HT films. The noncontinuous film morphology at lower P3HT thickness may be responsible for the charge trapping.

Thermal annealing has a more significant influence on the bias stress stability (Figure 5b). I_D for devices annealed at 60 °C (P3HT thickness = 50 nm) decreased by 70% after 1 h of bias stress, whereas devices annealed at higher temperatures (up to 150 °C) exhibited much less I_D decay; the device annealed at 120 °C showed only ∼6% decay after 1 h. It has been reported previously that thermal annealing of OTFTs leads to improvement of bias stability by reducing structural disorder.[23,24] The cause of improved bias stress resistance with annealing in the case of EGTs may be related to changes in P3HT film microstructure (e.g., enhanced crystallinity), or it may be due to removal of H_2O and solvent molecules from EGTs, which can serve as charge traps.[22,25]

Based on the optimization of the printed P3HT EGTs on SiO_2, we printed high-performance EGTs on flexible PET substrates for comparison (see Figure S6a in the SI). P3HT patches 50 nm thick were printed onto plastic substrates prepatterned with gold electrodes, and completed devices were annealed at 120 °C for 30 min. Figures S6b−d in the SI show the I_D−V_G and the I_D−V_D characteristics of a printed P3HT EGT on PET. The average saturation μ and V_{th} values were

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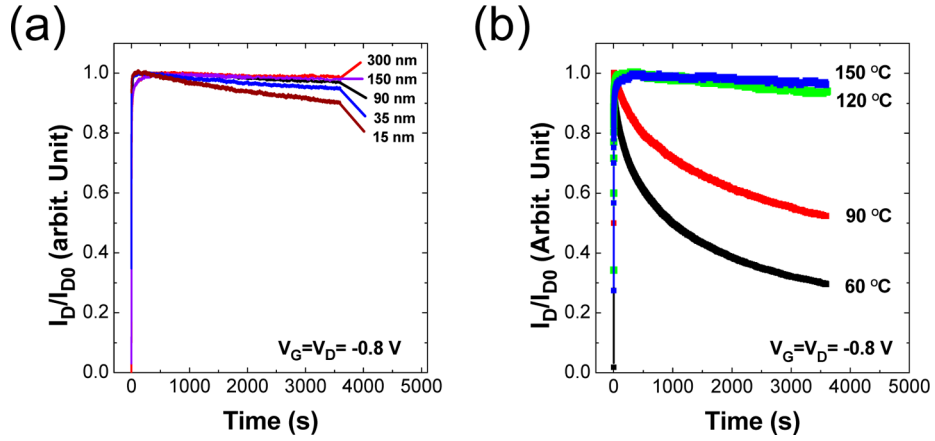

Figure 5. EGT response to bias stress. (a) Effect of film thickness: I_D versus time for EGTs on SiO_2 with different P3HT thicknesses and under bias stress with $V_G = V_D = -0.8$ V. All devices were annealed at 120 °C prior to testing. Time scale is 1 h. (b) Effect of annealing temperature: I_D versus time for P3HT EGTs on SiO_2 annealed at different temperatures under N_2 and then placed under bias stress with $V_G = V_D = -0.8$ V. All devices had the same P3HT film thickness of 50 nm.

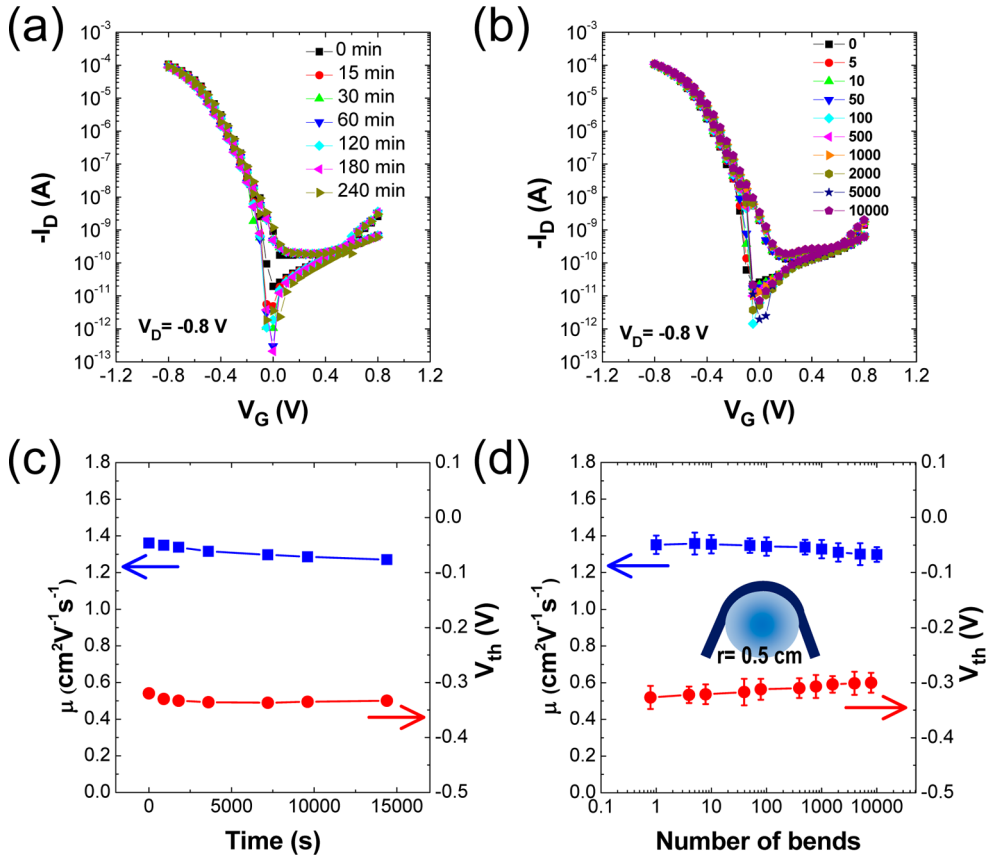

Figure 6. Response of flexible EGTs on plastic to bias stress and bending strain. The evolution of I_D–V_G transfer curves upon (a) applying sustained biases of $V_G = V_D = -0.8$ V over a period of 240 min (4 h) and (b) bending the substrate 10 000 times with a bending radius of 0.5 cm (1.5% strain). (c) Dependence of μ and V_{th} versus time extracted from panel (a). (d) μ and V_{th} versus number of bending cycles extracted from panel (b).

1.35 cm^2 V^{-1} s^{-1} and −0.34 V, respectively, and the overall device performance was comparable to EGTs on SiO_2.

Next, we investigated the operational stability of these flexible P3HT EGTs under both bias and repeated mechanical bending stress, separately. Devices either were exposed to sustained biases of $V_G = V_D = -0.8$ V over a period of 4 h for bias stress tests or were subjected to 10 000 repeated bends of the substrate. For the bending experiments, a bending radius (R) of 0.5 cm was employed, constituting a maximum tensile strain (ε) of 1.5% on the devices, according to $\varepsilon = D/2R$, where D = 150 μm is the plastic substrate thickness.[26] Figures 6a and 6b show the I_D–V_G curves of the flexible P3HT EGTs for bias and bending stress tests, and the variations of μ and V_{th} from these transfer curves are summarized in Figures 6c and 6d, respectively. Remarkably, for the bias stress tests, the decrease in μ over a period of 4 h was <10%, and the V_{th} shift (ΔV_{th}) was only −15 mV. For the mechanical stress tests, μ decreased by ~8% and V_{th} shifted by only +30 mV. These promising

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results might be further improved if the devices were printed on thinner plastic substrates and encapsulated such that the EGTs lay on the neutral strain plane.[27]

4. CONCLUSIONS

In conclusion, we have optimized the performance of aerosol-jet printed P3HT EGTs by controlling the P3HT thickness and the post-fabrication device annealing conditions. Relatively thin P3HT films (~50 nm) annealed at 120 °C have the best performance, in terms of the ON/OFF current ratio, threshold voltage, hysteresis, dynamic response, bias stress resistance, and mechanical durability. The optimized figures of merit for P3HT EGTs having channel W/L ratios of 500/25 are: ON/OFF current ratios of 10^6 with I_{OFF} $<10^{-10}$ A (or leakage $<10^{-6}$ A cm^{-2}), saturation hole mobilities of ~1.3 $cm^2 V^{-1} s^{-1}$, threshold voltages of −0.3 V, and subthreshold swings of 70 mV $decade^{-1}$. Ongoing work aims to incorporate these devices in printed, flexible circuits for biosensing applications.

■ ASSOCIATED CONTENT

Ⓢ Supporting Information

Supporting information has been provided on the following topics: I_G-V_G characteristics obtained at different gate sweeping rates for 50-nm-thick P3HT EGT; I_D-V_G transfer curves for the printed EGTs on SiO_2 substrate with different P3HT thicknesses; surface morphologies and cross sections for the printed P3HT films on SiO_2 substrate characterized by AFM; log I_D-V_G transfer curves at different device annealing temperatures for printed EGTs with different P3HT thicknesses; and the thickness change of P3HT films, depending on thermal annealing. Additional figures (PDF). This material is available free of charge via the Internet at http://pubs.acs.org.

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Notes

The authors declare no competing financial interest.

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■ REFERENCES

(1) Lodge, T. P. *Science* **2008**, *321*, 50−51.
(2) Facchetti, A. *Nat. Mater.* **2008**, *7*, 839−840.
(3) Cho, J. H.; Lee, J.; Xia, Y.; Kim, B.; He, Y.; Renn, M. J.; Lodge, T. P.; Frisbie, C. D. *Nat. Mater.* **2008**, *7*, 900−906.
(4) Hamedi, M.; Herlogsson, L.; Crispin, X.; Marcilla, R.; Berggren, M.; Inganas, O. *Adv. Mater.* **2009**, *21*, 573−577.
(5) Lu, A.; Dai, M.; Sun, J.; Jiang, J.; Wan, Q. *IEEE Electron Device Lett.* **2011**, *32*, 518−520.
(6) Dasgupta, S.; Kruk, R.; Mechau, N.; Hahn, H. *ACS Nano* **2011**, *5*, 9628−9638.
(7) Herlogsson, L.; Noh, Y. Y.; Zhao, N.; Crispin, X.; Sirringhaus, H.; Berggren, M. *Adv. Mater.* **2008**, *20*, 4708−4713.
(8) Ye, J. T.; Inoue, S.; Kobayashi, K.; Kasahara, Y.; Yuan, H. T.; Shimotani, H.; Iwasa, Y. *Nat. Mater.* **2010**, *9*, 125−128.
(9) Yang, S. Y.; Cicoira, F.; Byrne, R.; Benito-Lopez, F.; Diamond, D.; Owens, R. M.; Malliaras, G. G. *Chem. Commun.* **2010**, *46*, 7972−7974.
(10) Lin, P.; Luo, X. T.; Hsing, I. M.; Yan, F. *Adv. Mater.* **2011**, *23*, 4035−4040.
(11) Xia, Y.; Zhang, W.; Ha, M. J.; Cho, J. H.; Renn, M. J.; Kim, C. H.; Frisbie, C. D. *Adv. Funct. Mater.* **2010**, *20*, 587−594.
(12) Xia, Y.; Frisbie, C. D. In *Organic Electronics II: More Materials and Applications*; Klauk, H., Ed.; Wiley−VCH Verlag GmbH & Co. KGaA: Weinheim, Germany, 2012; pp 199−233.
(13) Kim, S. H.; Hong, K.; Xie, W.; Lee, K. H.; Zhang, S.; Lodge, T. P.; Frisbie, C. D. *Adv. Mater.* **2013**, *25*, 1822−1846.
(14) Hong, K.; Kim, S. H.; Lee, K. H.; Frisbie, C. D. *Adv. Mater.* **2013**, *25*, 3413−3418.
(15) Lee, J.; Kaake, L. G.; Cho, J. H.; Zhu, X. Y.; Lodge, T. P.; Frisbie, C. D. *J. Phys. Chem. C* **2009**, *113*, 8972−8981.
(16) Ogawa, S.; Kimura, Y.; Ishii, H.; Niwano, M. *Jpn. J. Appl. Phys.* **2003**, *42*, L1275−L1278.
(17) Ogawa, S.; Naijo, T.; Kimura, Y.; Ishii, H.; Niwano, M. *Synth. Met.* **2005**, *153*, 253−256.
(18) Sze, S. M. *Physics of Semiconductor Devices*; Wiley: New York, 1981.
(19) Abdou, M. S. A.; Orfino, F. P.; Son, Y.; Holdcroft, S. *J. Am. Chem. Soc.* **1997**, *119*, 4518.
(20) Hwang, D. K.; Lee, K.; Im, S.; Park, J. H.; Kim, E. *Appl. Phys. Lett.* **2006**, *89*, 093507 (1−3)..
(21) Kim, S. H.; Yun, W. M.; Kwon, O.-K.; Hong, K.; Yang, C.; Choi, W.-S.; Park, C. E. *J. Phys. D: Appl. Phys.* **2010**, *43*, 465102-1−465102-8.
(22) Sirringhaus, H. *Adv. Mater.* **2009**, *21*, 3859−3873.
(23) Choi, H. H.; Kang, M. S.; Kim, M.; Kim, A.; Cho, J. H.; Cho, K. *Adv. Funct. Mater.* **2013**, *23*, 690−696.
(24) Fukuda, K.; Yokota, T.; Kuribara, K.; Sekitani, T.; Zschieschang, U.; Klauk, H.; Someya, T. *Appl. Phys. Lett.* **2010**, *96*, 053302-1−053302-3.
(25) Choi, H. H.; Lee, W.; Cho, K. *Adv. Funct. Mater.* **2012**, *22*, 4833−4839.
(26) Sekitani, T.; Kato, Y.; Iba, S.; Shinaoka, H.; Someya, T.; Sakurai, T.; Takagi, S. *Appl. Phys. Lett.* **2005**, *86*, 073511-1−073511-3.
(27) Sekitani, T.; Zschieschang, U.; Klauk, H.; Someya, T. *Nat. Mater.* **2010**, *9*, 1015−1022.